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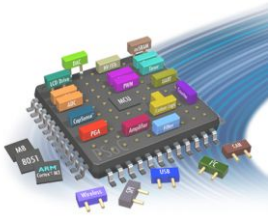
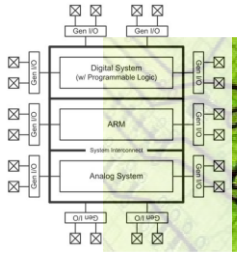
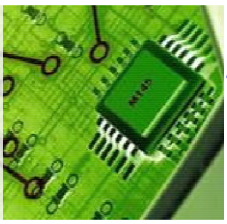
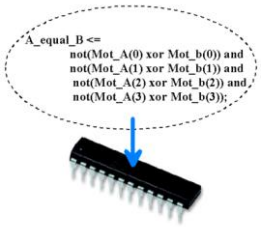






PSOC Les blocs logiques configurables UDB

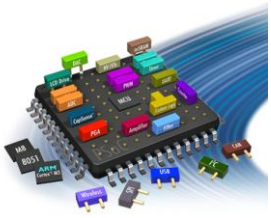
Universal Digital Blocks

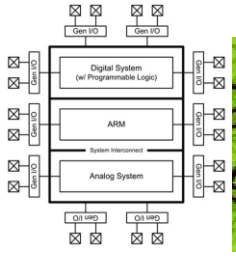


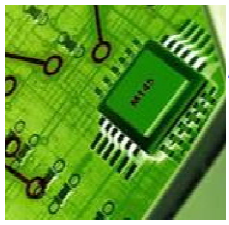
Initiation à la logique programmable des UDB du PSoC

📖 PSoC5-LP.pdf 446 pages

STI2D SIN



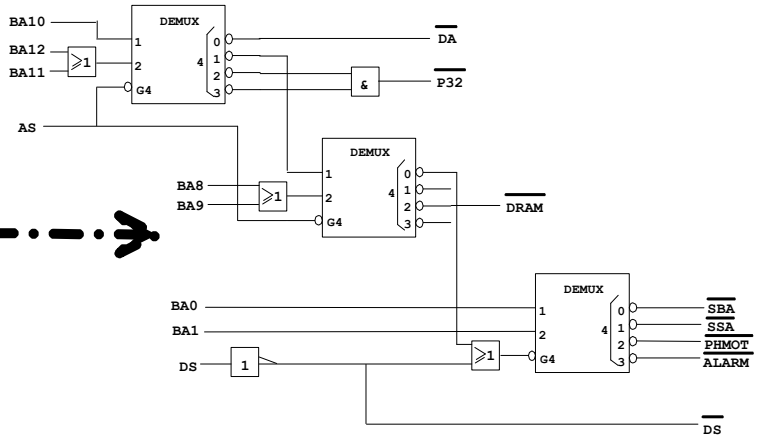


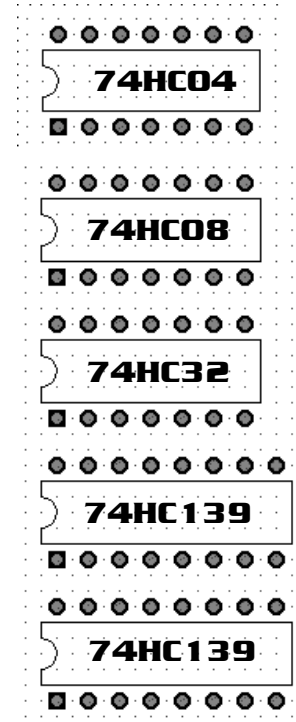


1 Introduction à la logique programmable

Synthèse d'un schéma logique complexe :

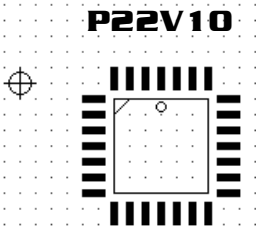
Du schéma





DECODAGE AVEC DES BOITIERS DE LOGIQUE COMBINATOIRE

Vers le PAL



DECODAGE AVEC UN UNIQUE BOITIER DE LOGIQUE PROGRAMMABLE

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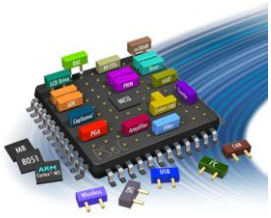
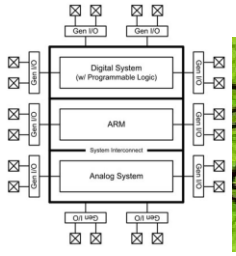
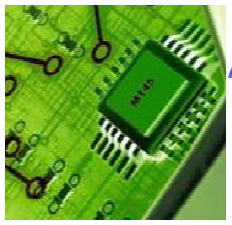
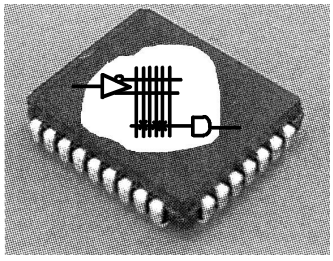





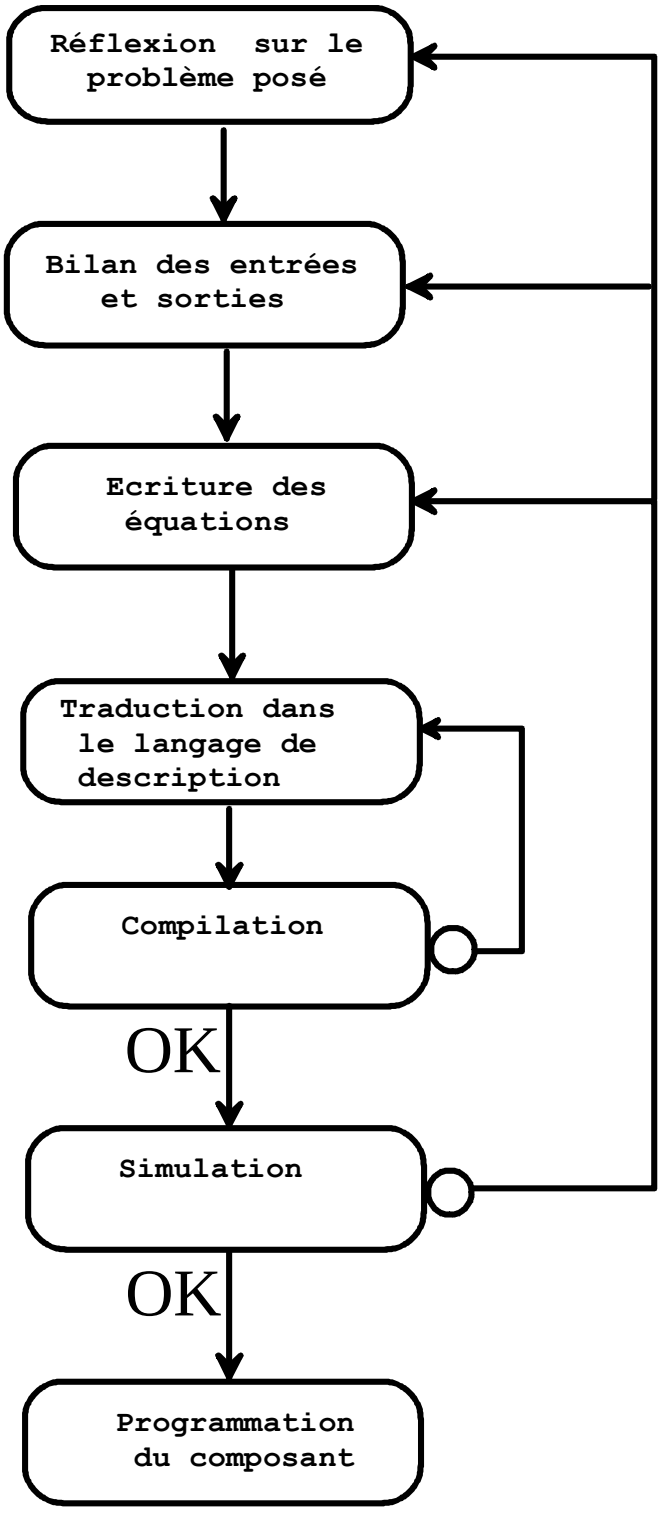
Principe de la synthèse

Projet

VHDL
VERILOG



Composant



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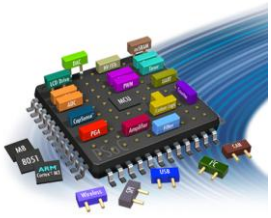
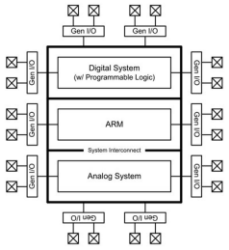
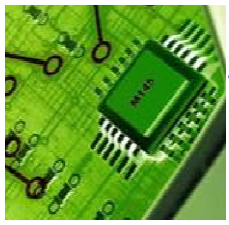
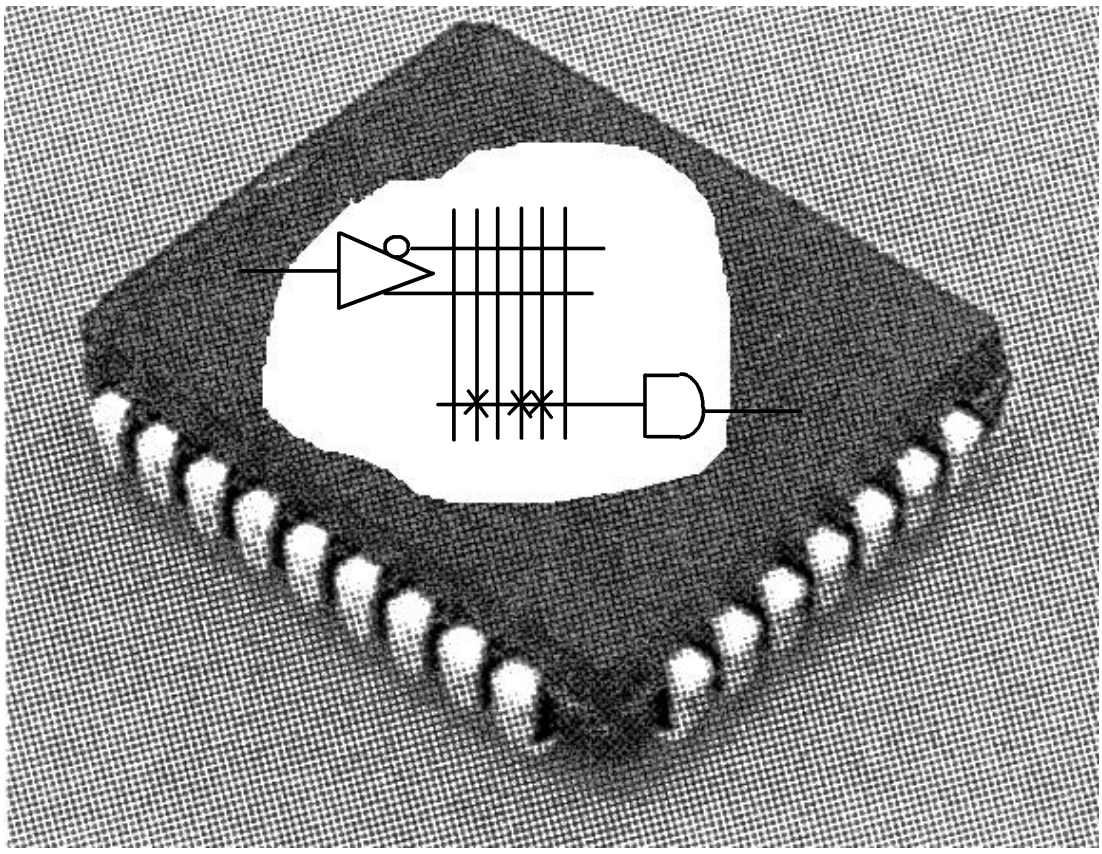






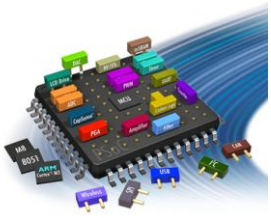
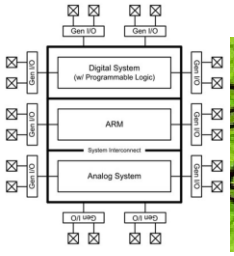
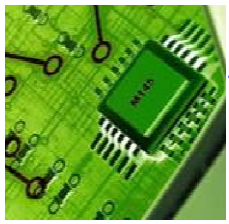
Un seul composant



=> contient de multiples équations logiques

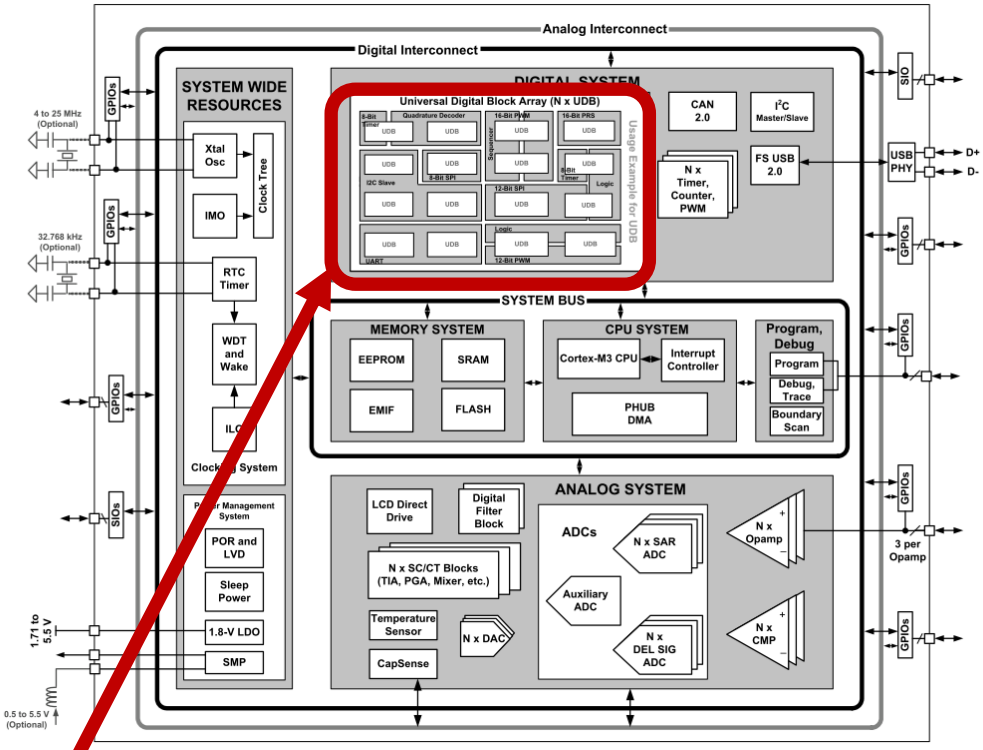
=> remplace plusieurs composants traditionnels

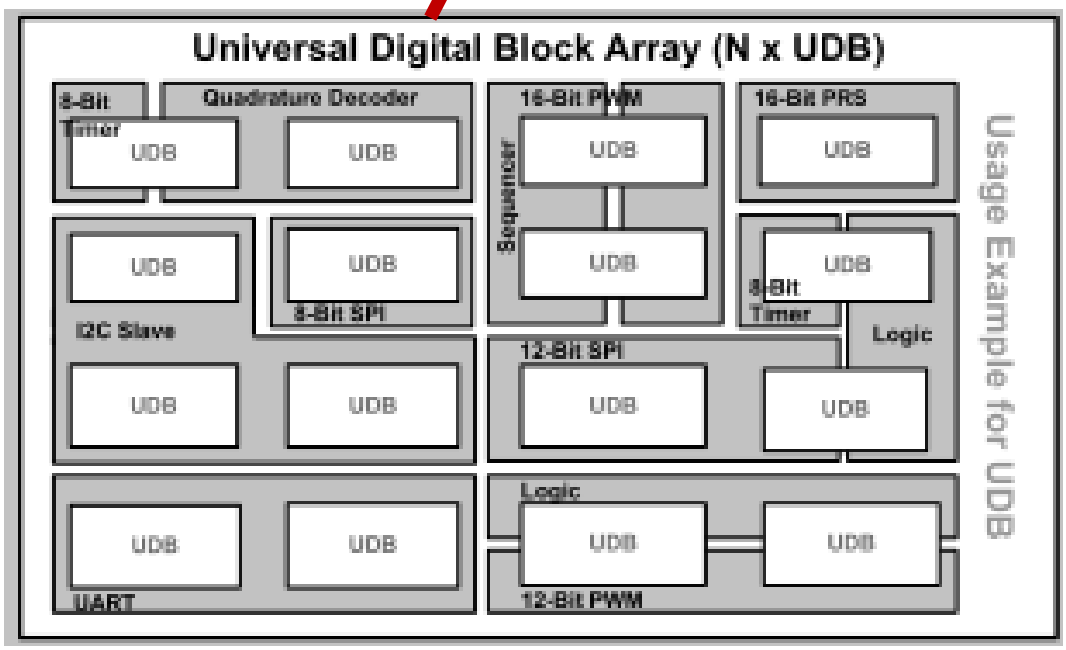
STI2D SIN

2 La logique programmable dans les PSoC

Universal Digital Blocks





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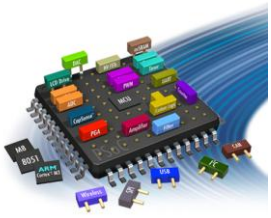
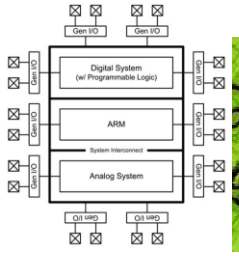
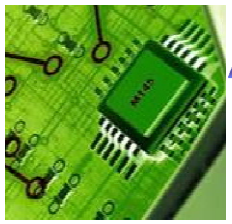
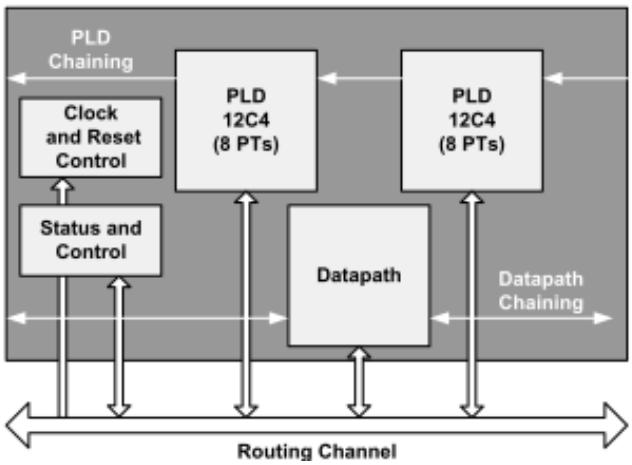





3 Description d'un UDB

- For optimal flexibility, each UDB contains several components:
  - ALU-based 8-bit datapath (DP) with an 8-word instruction store and multiple registers and FIFOs
  - Two PLDs, each with 12 inputs, eight product terms and four macrocell outputs
  - Control and status modules
  - Clock and reset modules
- PSoC 5LP contains an array of up to 24 UDBs
- Flexible routing through the UDB array
- Portions of UDBs can be shared or chained to enable larger functions
- Flexible implementations of multiple digital functions, including
  - timers,
  - counters,
  - PWM (with dead band generator),
  - UART,
  - I2C,
  - SPI,
  - and CRC generation/checking

Figure 21-1. UDB Block Diagram



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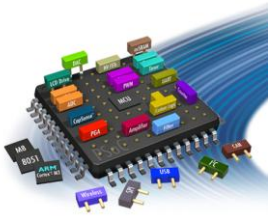
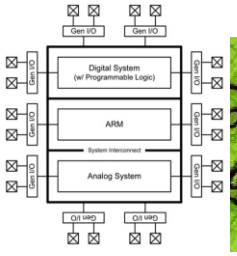
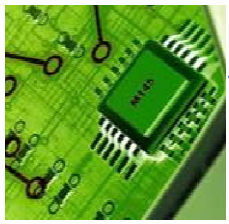
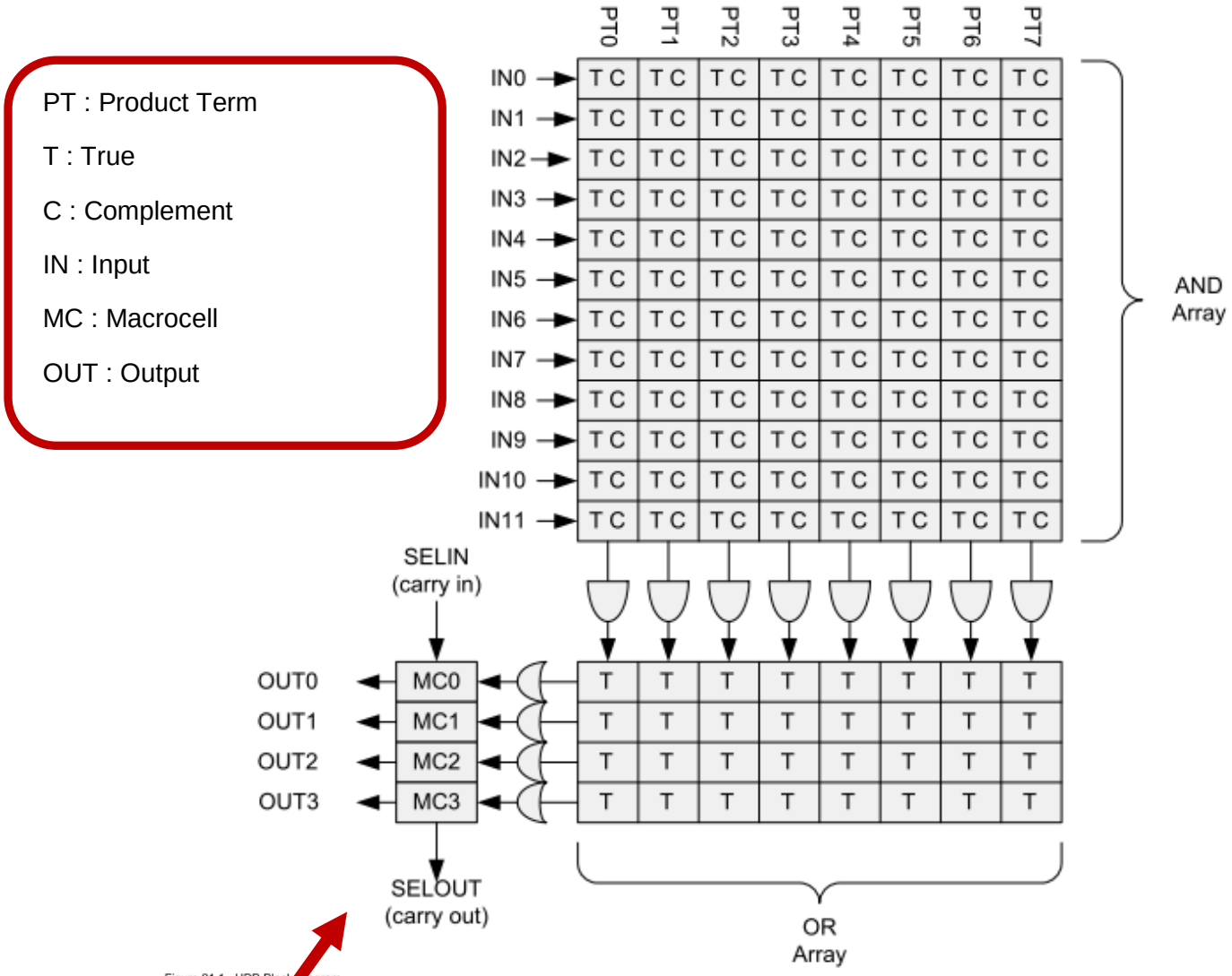
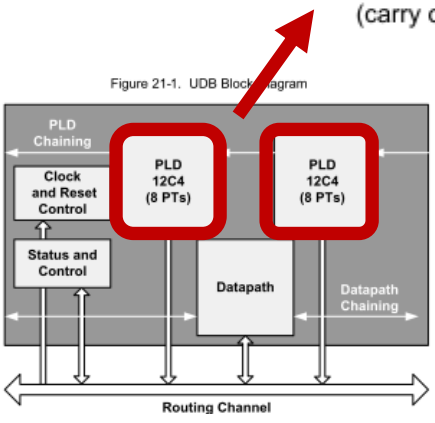




Structure d'un **P**rogrammable **L**ogic **D**evice

Figure 21-2. PLD 12C4 Structure





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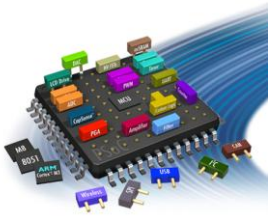
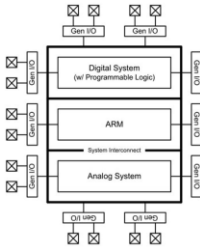
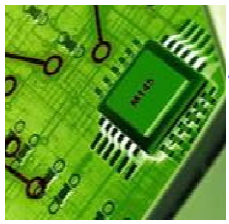




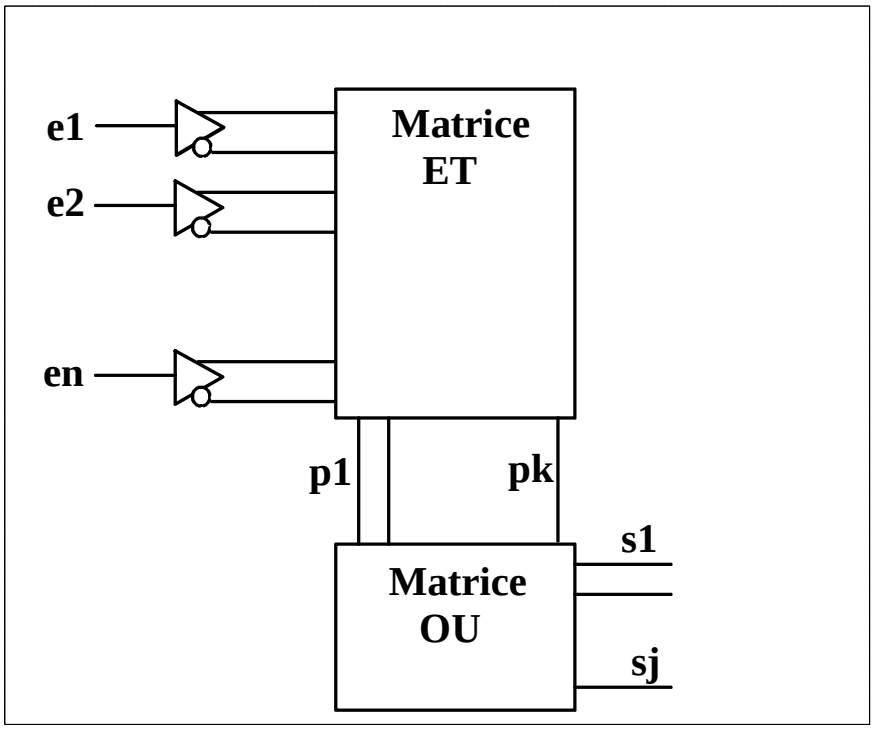
4 Implantation d'une équation logique dans un PLD de type PAL16H4 (le plus simple des PAL et CPLD)

Forme générale d'une équation logique :

$$F = b.\overline{c}.d + \overline{e}.f.d + \overline{a}.g$$

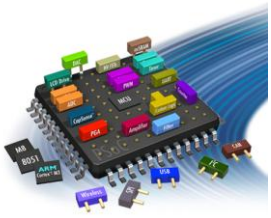
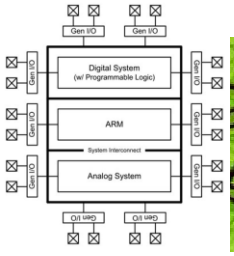
Somme de produits

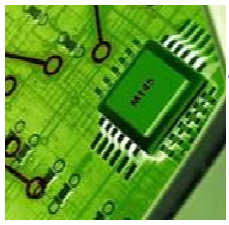
Structure générale d'un Pal :



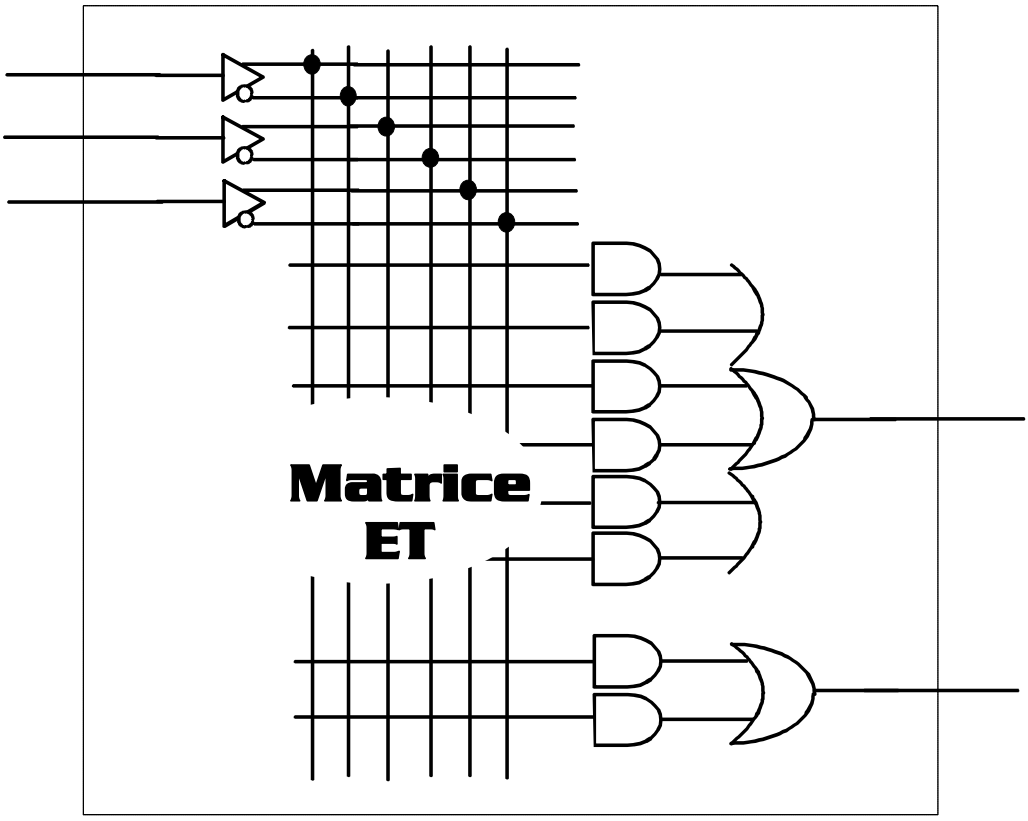
Somme de produits

STI2D SIN




Structure générale d'un Pal :

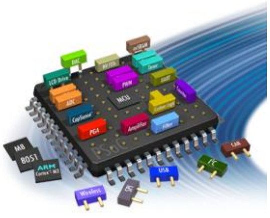


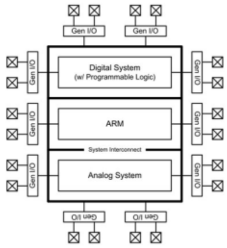
Bilan :

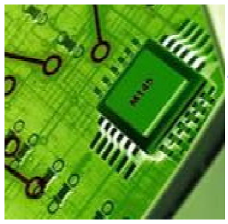
=> nombre d'entrées

=> nombre de sorties

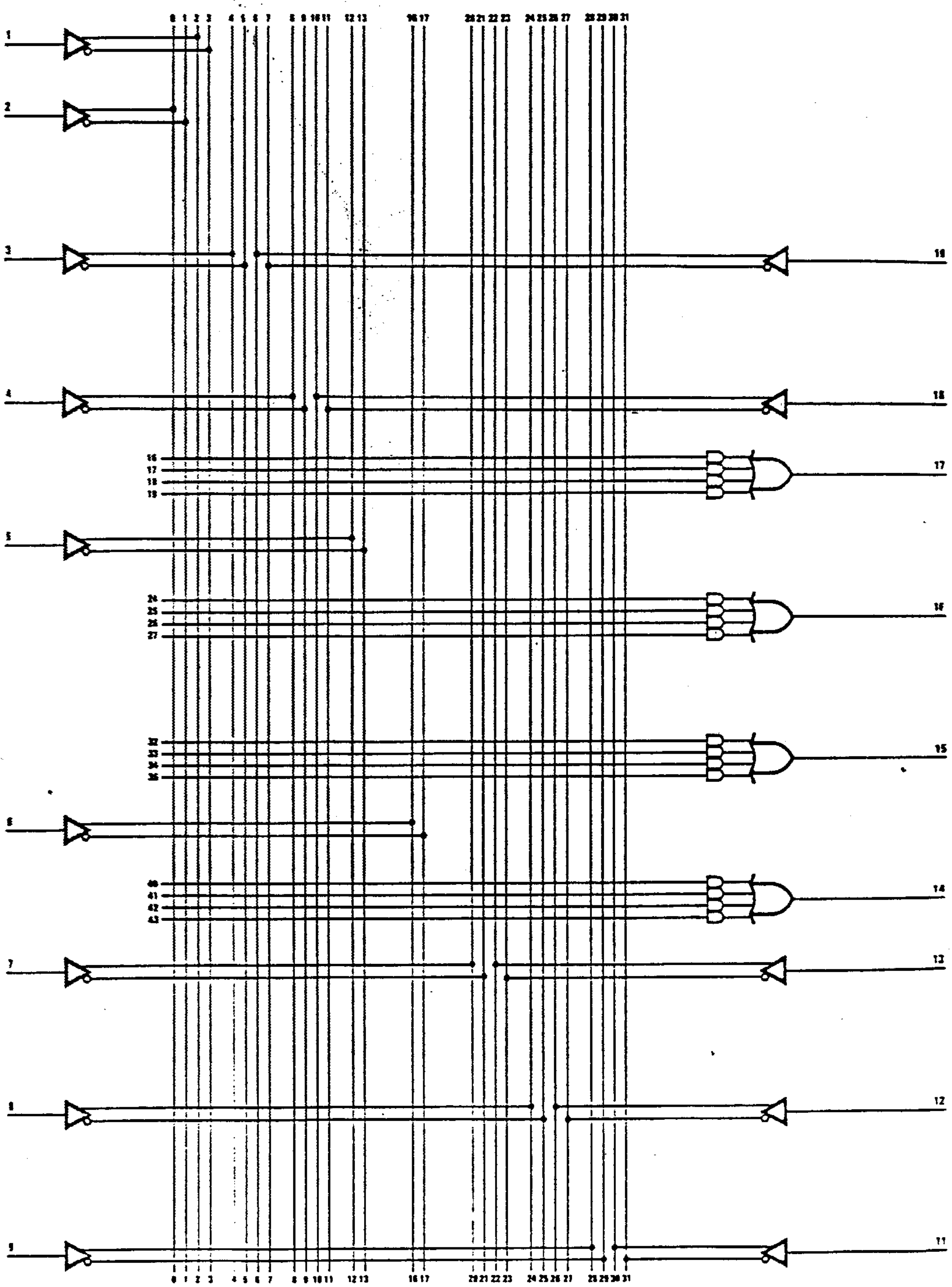
=> nombre de termes porduits/sortie







Logic Diagram **14H4**



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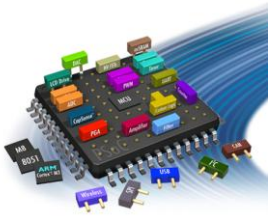
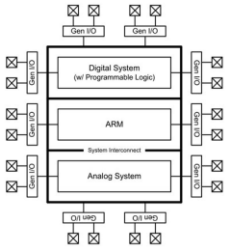
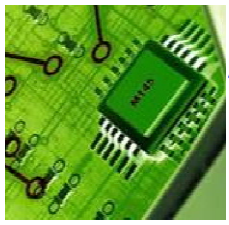


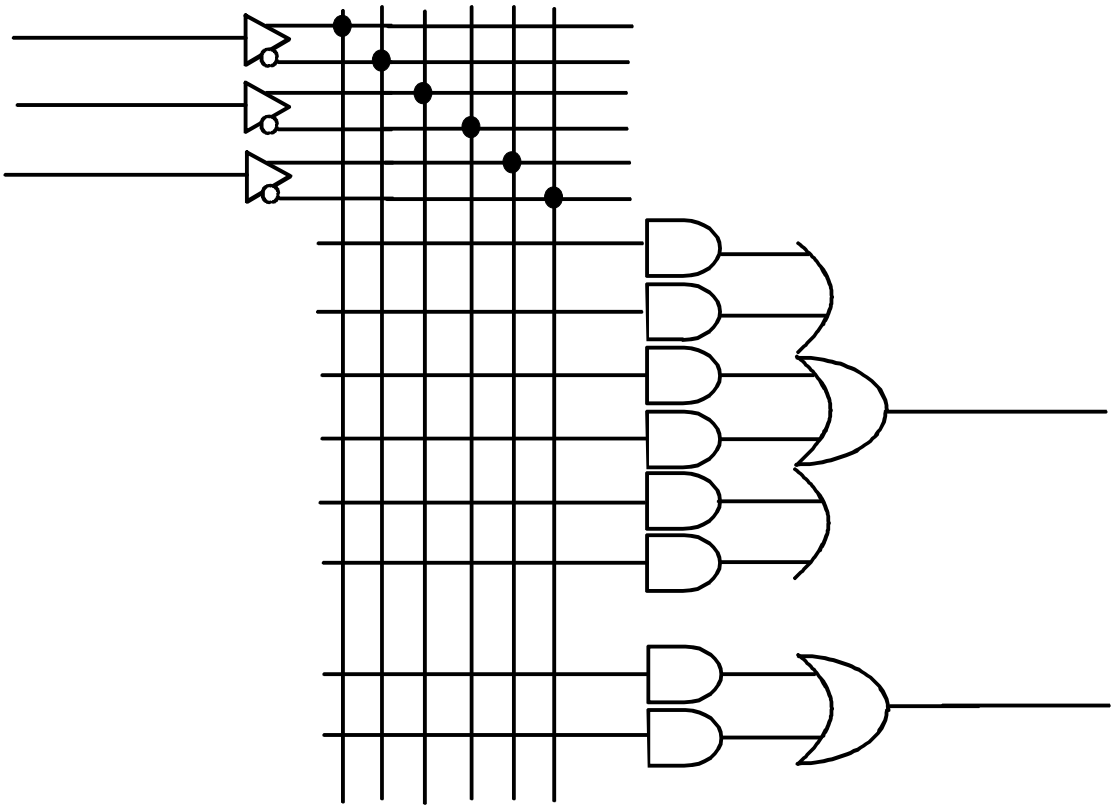




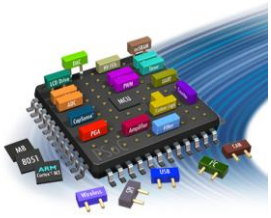
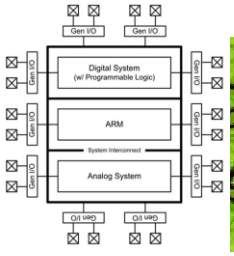
5 Exercices d'implantation

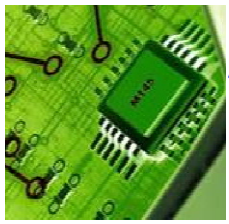
5.1 Exemple n° 1 :

$$F = \overline{b}.c.d \qquad G = b + c.\overline{d}$$



STI2D SIN

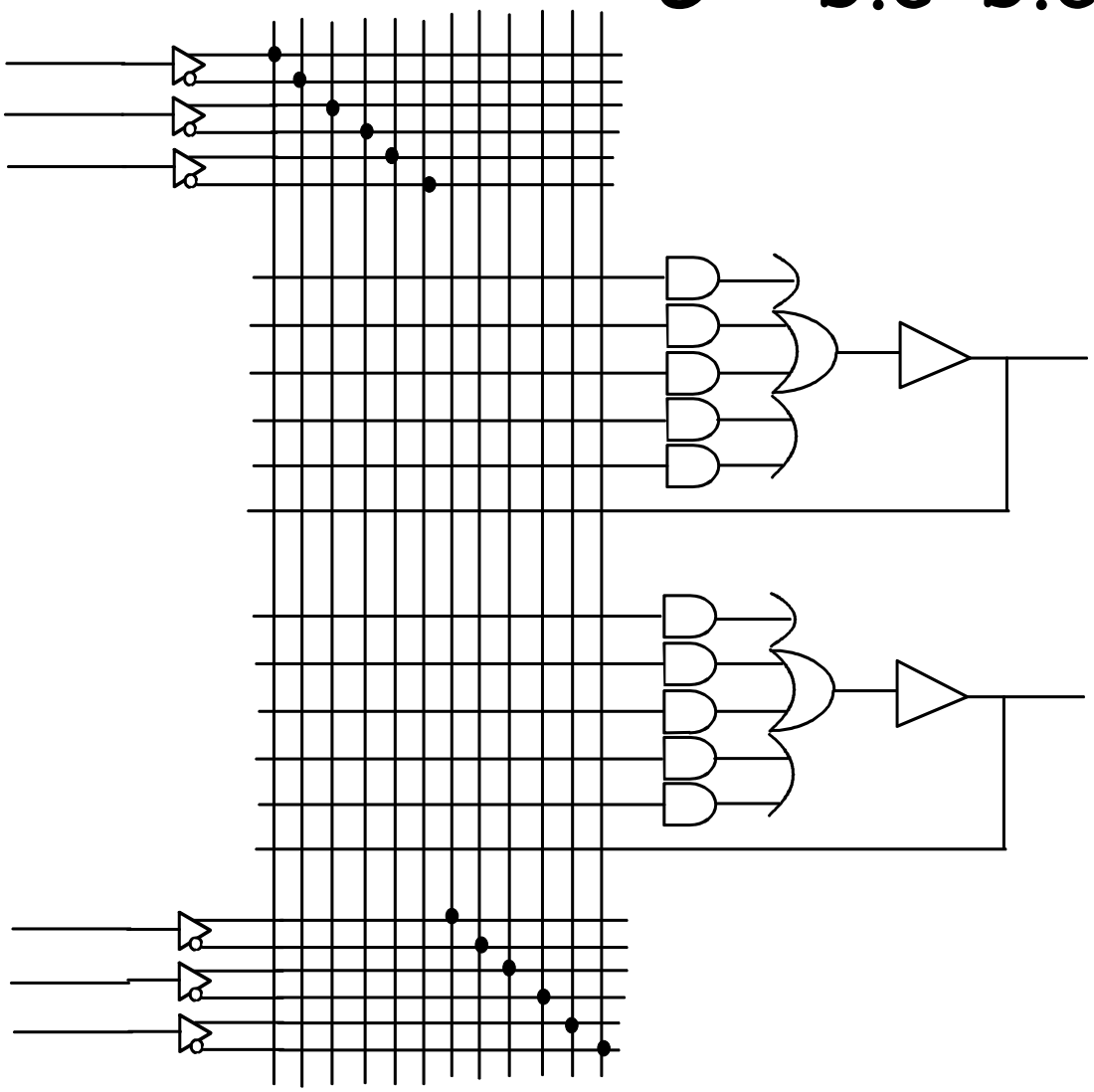






5.2 Exemple n° 2 :

$$F = \overline{b}.\overline{c}.d + a.\overline{d}$$

$$G = \overline{b}.\overline{c} + b.c$$



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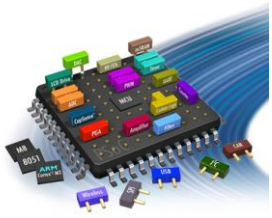
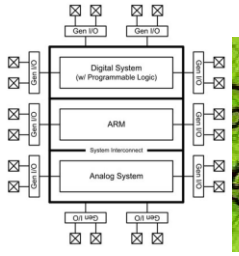
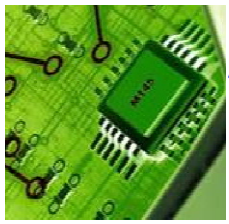
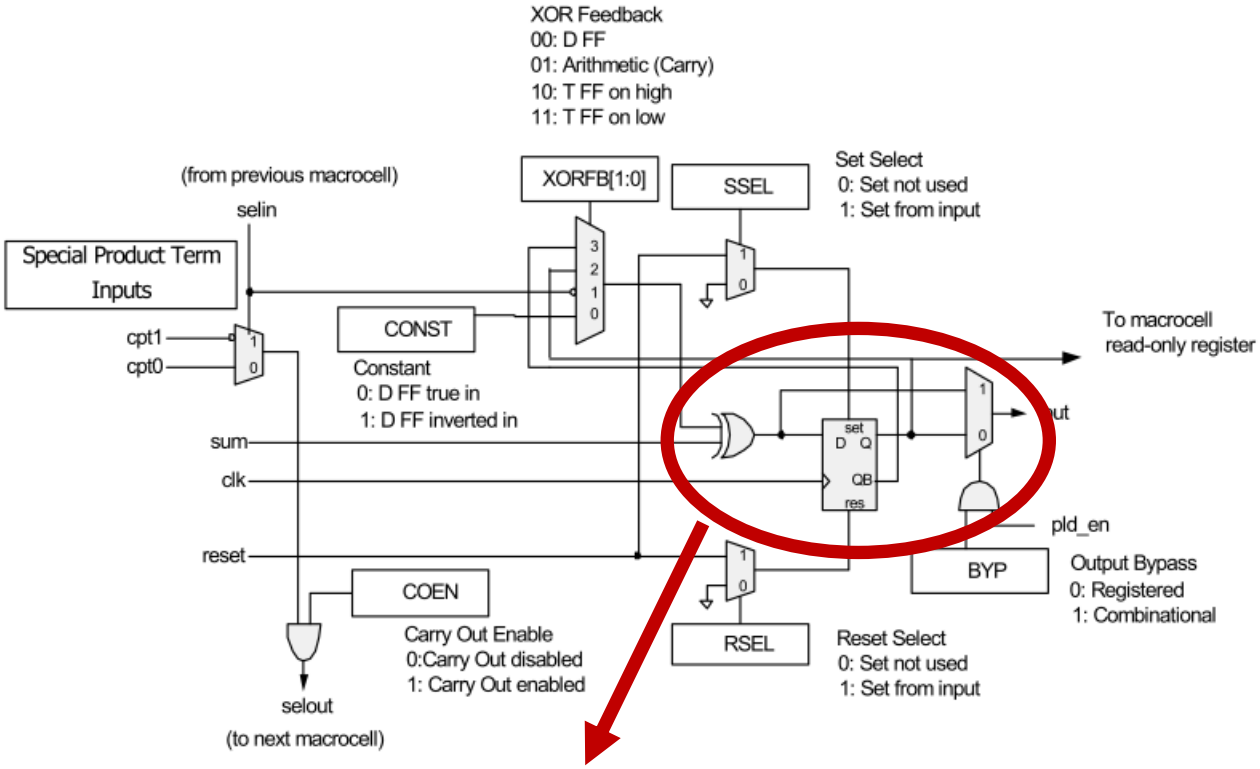
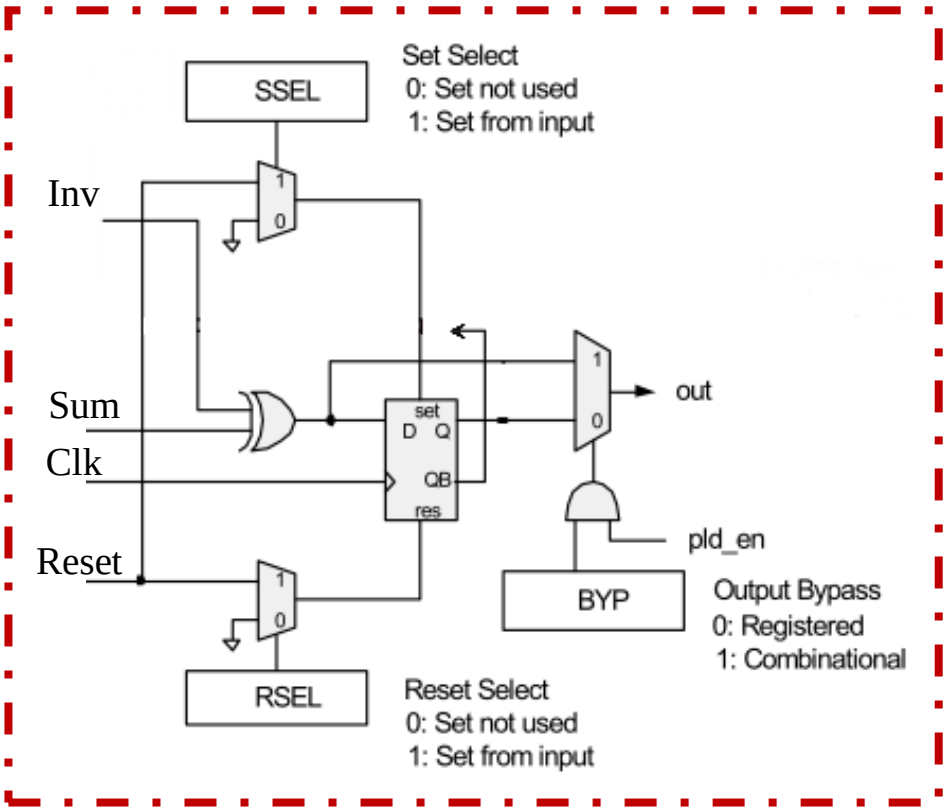




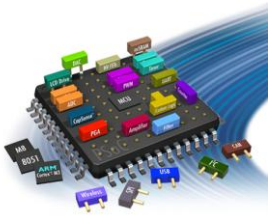
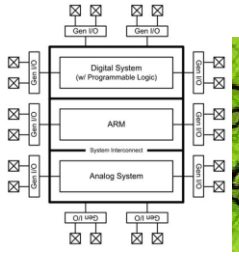
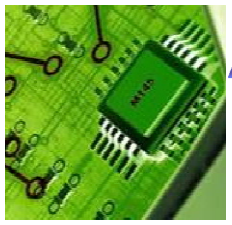
6 Description de la Macrocellule de l'UDB

La macrocellule implante l'équation soit en logique combinatoire soit en logique séquentielle, dans ce dernier cas une bascule D est utilisée pour mémorisée un résultat sur un bit. La génération de schéma de logique séquentielle est possible, comptage, mémoires, machines d'états ...





STI2D SIN

7 Le bloc Datapath

Figure 21-1. UDB Block Diagram

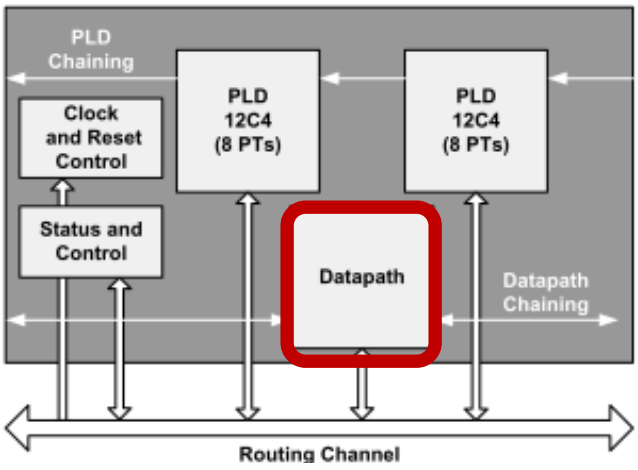
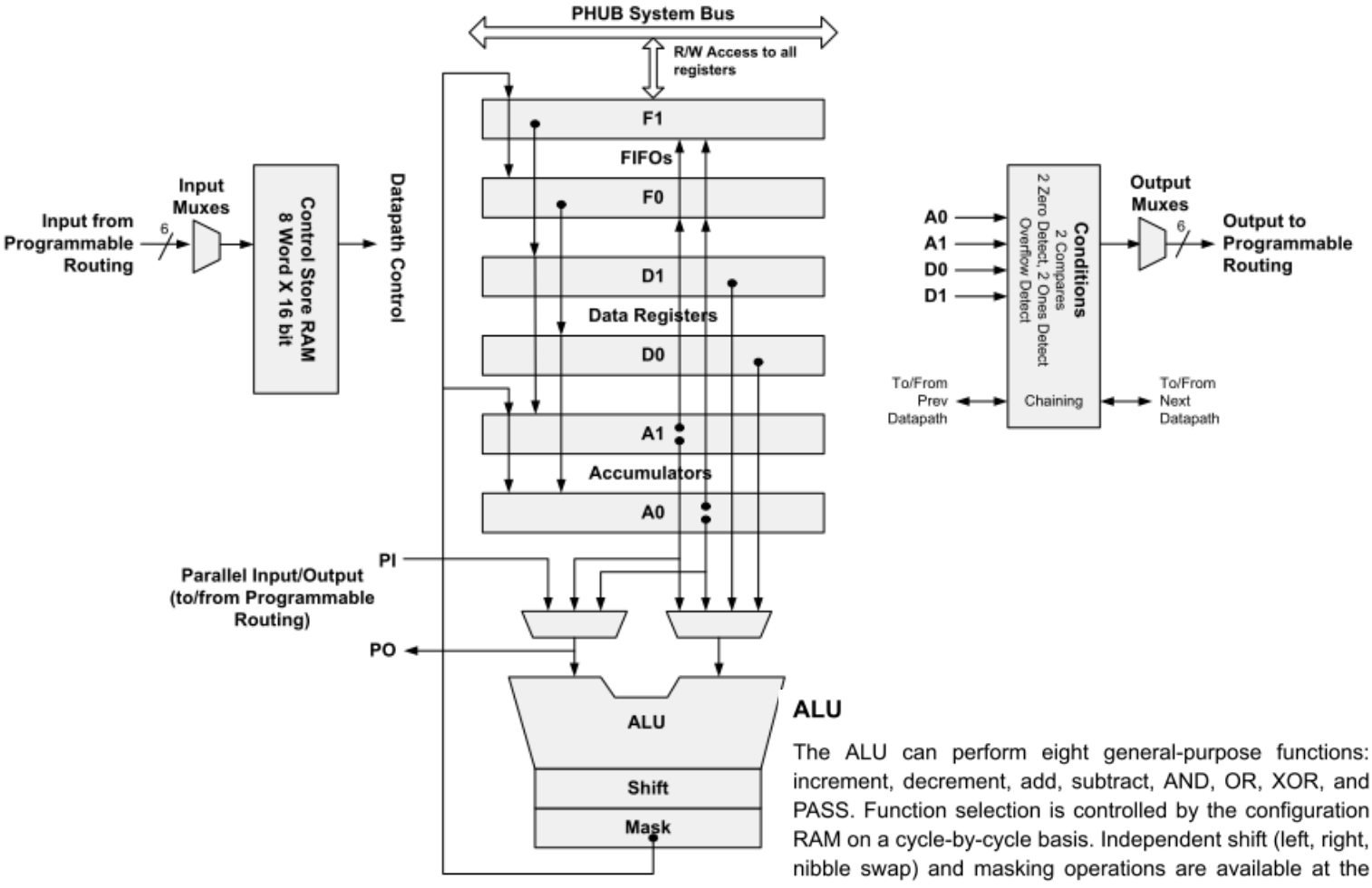


Figure 21-6. Datapath Top Level



ALU

The ALU can perform eight general-purpose functions: increment, decrement, add, subtract, AND, OR, XOR, and PASS. Function selection is controlled by the configuration RAM on a cycle-by-cycle basis. Independent shift (left, right, nibble swap) and masking operations are available at the output of the ALU.